

#4 242-01 6-AU 2812



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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/729,154 12/04/00

C.H. Yu, S.M. Jang

A SHALLOW TRENCH ISOLATION PROCESS
FOR REDUCED JUNCTION LEAKAGE

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,447,884 to Fahey et al, "Shallow Trench
Isolation With Thin Nitride Liner", describes a method of
forming shallow trench isolation with a nitride liner layer for
devices in integrated circuits which solves a problem of
recessing the nitride liner that led to unacceptable voids in
hte trench filler material by using a liner thickness of less
than 5 nm.


U.S. Patent 5,316,965 to Philipossian et al, "Method Of Decreasing The Field Oxide Etch Rate In Isolation Technology", discloses an improved process for planarizing an isolation barrier in the fabrication of an integrated circuit on a semiconductor substrate.

U.S. Patent 5,208,179 to Okazawa, "Method Of Fabricating Programmable Read Only Memory Device Having Trench Isolation Structure", teaches a method of fabricating a semiconductor integrated circuit such as a programmable read only memory (PROM) cell.

U.S. Patent 5,112,772 to Wilson et al, "Method Of Fabricating A Trench Structure", discloses a method of fabricating a trench structure. The semiconductor has a silicon dioxide layer, a polysilicon layer, and a silicon nitride layer formed on its surface.

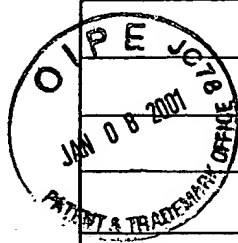
U.S. Patent 5,492,858 to Bose et al, "Shallow Trench Isolation Process For High Aspect Ratio Trenches", discloses a method of planarizing the surface of a silicon wafer in integrated circuit manufacture where shallow trench isolation techniques are employed.

Sincerely,


Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i>	Docket Number (Optional) TSMC-97-510B	Application Number 09729,154
	Applicant C.H. Yu et al	
	Filing Date 12/4/00	Group Art Unit 2812

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5208179	5/4/93	Okazawa	437	52	12/27/90
	5492858	2/20/96	Bose et al	437	67	4/20/94
	5112772	5/12/92	Wilson et al	437	67	9/27/91
	5316965	5/31/94	Philipossian et al	437	70	7/29/93

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

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EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.